Amendments to the Claims

1. (Original) A semiconductor chip containing an embedded macro, said macro containing a plurality of slices extending therethrough, wherein each slice has its own porosity factor representing the number of open channels extending through the slice, each channel containing a circuit wire passing through the slice for the delivery of signals within the chip.

2. (Original) The chip according to claim 1 wherein the embedded macro is a densely obstructed macro.

3. (Original) The chip according to claim 2 wherein the macro is a field programmable gate array.

4. (Original) The chip according to claim 1 wherein the porosity of each slice is independent of its functionality.

5. (Original) The chip according to claim 4 wherein each slice corresponds to a timing allocation in the semiconductor chip.

6. (Original) The chip according to claim 4 wherein each slice contains a plurality of blocks, the height of blocks in a horizontal slice being generally the same, as is the width of blocks within a vertical slice.

7. (Original) A method for improving the routing of signals through an array macro embedded in a semiconductor chip wherein the macro comprises a plurality of slices, each having different porosities depending on the number of channels extending therethrough, the method comprising the steps of:

(a) developing a chip floor plan including early timing allocation and proposed array placement;

(b) flagging critical logical wiring nets and overlaying the floor plan with the nets;

(c) making an initial selection of slices for the macro based upon the number of channels required at each location within the macro; and

(d) assembling the macro with the placement of slices to provide porosities based upon the channel requirements.

8. (Original) The method according to claim 7 wherein the slices are composed of a plurality of functional blocks wherein blocks with the same functionality have the same mass.

9. (Original) The method according to claim 7 wherein the step of chip floor planning includes establishing a base level of porosity in the chip.

10. (Original) The method according to claim 7 wherein the array comprises a field programmable gate array.

11. (Original) The method according to claim 7 including the further step of changing slices after floor planning to make further adjustments in porosity.

12. (Original) The method according to claim 11 wherein the changes occur during the execution phase of chip design prior to chip construction.

13. (Original) A macro for use in a field programmable gate array embedded in a semiconductor chip, said macro containing a plurality of slices, each of which has a unique porosity factor representing channels within the slice, the slices positioned at locations within the chip wherein the number of channels in each slice corresponds to the number of circuits in the chip that are intended to pass through the macro at each location.

14. (Original) The macro according to claim 13 wherein each of the slices is pre-wired before it is assembled into the macro.

15. (Original) The macro according to claim 13 wherein each of the slices is composed of a plurality of functional blocks.

16. (Original) The macro according to claim 15 wherein the mass of each of the blocks is the same.

17. (Original) The macro according to claim 14 wherein the size of each slice corresponds to the degree of porosity of the slice.

18. (Original) The macro according to claim 16 wherein the length of the wires within a slice is matched to the length of the channels therein.

19. (Original) The macro according to claim 18 wherein the wires are lengthened with spacer tiles.

20. (Original) The macro according to claim 18 wherein the wires are lengthened by splicing an insert into each wire

21. (Withdrawn) An article of manufacture comprising a medium having a computer readable program embodied in said medium, wherein the computer readable program, when executed on a computer, causes the computer to:

(a) develop a chip floor plan including early timing allocation and proposed gate array placement;

(b) flag critical logical wiring nets and overlay the floor plan with the nets;

(c) make an initial selection of slices for the macro based upon the required number of channels required at each location within the macro; and

(d) assemble the macro with the placement of slices based upon the channel requirements.

22. (Withdrawn) The article according to claim 21 wherein the program causes the computer to establish a base level of porosity in the chip during the step of chip floor planning.

23. (Withdrawn) The article according to claim 22 wherein the program causes the computer to make further changes in slices after the step of floor planning to accommodate changes in channel requirements.